Exhibit 5

Claims Reciting Specific "Bits" Of A PCI Bus Transaction, Including But Not Limited To "Address Bits," "Data Bits," And "Byte Enabled Information Bits"

Claim Limitations	Asserted Claims
"**address and data bits** of a Peripheral Component Interconnect (PCI) bus transaction"	'768 patent, claims 1, 4, 7, 9, 10, 13, 15, 18, 22, 30, 33, 39; '750 patent, claims 5, 10, 18, 31, 35, 46; '797 patent, claims 7, 10, 14, 36; '359 patent, claims 3, 7, 17; '977 patent, claims 1, 9, 10, 16; '654 patent, claim 14; '739 patent, claims 29, 31; '602 patent, claim 14; '140 patent, claim 30; '468 patent, claims 14, 26, 29, 35, 37, 45; '947 patent, claims 54, 57.
"**address and data bits** of a Peripheral Component Interconnect (PCI) bus transaction **with different serialized forms**"	'768 patent, claim 8.
"**address bits, data bits, and byte enable information bits** of a Peripheral Component Interconnect (PCI) bus transaction"	'750 patent, claims 1, 18, 21, 25, 27, 29, 44; '947 patent, claims 19, 35, 48, 51.